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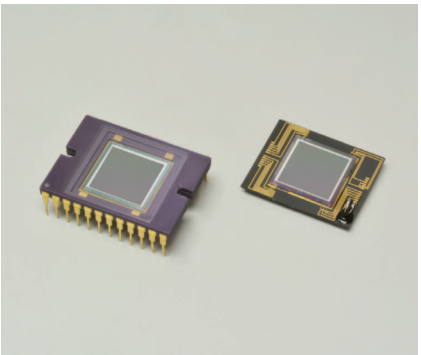
CCD area image sensors



S9736 series

512 × 512 pixels, front-illuminated FFT-CCDs

The S9736 series is a family of FFT-CCD area image sensors specifically designed for low-light-level detection in scientific applications. The S9736 series also features low noise and low dark current (MPP mode operation). These enable low-light-level detection and long integration time, thus achieving a wide dynamic range.
Two different packages (ceramic DIP, plate type) are provided.

Features

- **512 (H) × 512 (V) pixel format**
- **Pixel size: 24 × 24 µm**
- **100 % fill factor**
- **Wide dynamic range**
- **Low dark current**
- **Low readout noise**
- **MPP operation**
- **2 types of packages are available**

Applications

- **Astronomy**
- **Scientific measuring instrument**
- **Fluorescence spectrometer**
- **Raman spectrophotometer**
- **Optical and spectrophotometric analyzer**
- **For low-light-level detection requiring**

Structure

Parameter	S9736-01	S9736-03
CCD structure	Full frame transfer	
Fill factor	100 %	
Number of active pixels	512 (H) × 512 (V)	
Pixel size	24 (H) × 24 (V) µm	
Active area	12.288 (H) × 12.288 (V) mm	
Vertical clock phase	2-phase	
Horizontal clock phase	2-phase	
Output circuit	One-stage MOSFET source follower	
Cooling	Non-cooled	
Package	24-pin ceramic DIP	Plate type
Window	None	

Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+50	°C
Storage temperature	Tstg	-50	-	+70	°C
Output transistor drain voltage	VOD	-0.5	-	+25	V
Reset drain voltage	VRD	-0.5	-	+18	V
Test point (vertical input source)	VISV	-0.5	-	+18	V
Test point (horizontal input source)	VISH	-0.5	-	+18	V
Test point (vertical input gate)	VIG1V, VIG2V	-15	-	+15	V
Test point (horizontal input gate)	VIG1H, VIG2H	-15	-	+15	V
Summing gate voltage	VSG	-15	-	+15	V
Output gate voltage	VOG	-15	-	+15	V
Reset gate voltage	VRG	-15	-	+15	V
Transfer gate voltage	VTG	-15	-	+15	V
Vertical shift register clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal shift register clock voltage	VP1H, VP2H	-15	-	+15	V

Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		VOD	18	20	22	V
Reset drain voltage		VRD	12	13	14	V
Output gate voltage		VOG	-0.5	2	-	V
Substrate voltage		VSS	-	0	-	V
Test point (vertical input source)		VISV	-	VRD	-	V
Test point (horizontal input source)		VISH	-	VRD	-	V
Test point (vertical input gate)		VIG1V, VIG2V	-8	0	-	V
Test point (horizontal input gate)		VIG1H, VIG2H	-8	0	-	V
Vertical shift register clock voltage	High	VP1VH, VP2VH	0	3	6	V
	Low	VP1VL, VP2VL	-9	-8	-7	
Horizontal shift register clock voltage	High	VP1HH, VP2HH	0	3	6	V
	Low	VP1HL, VP2HL	-9	-8	-7	
Summing gate voltage	High	VSGH	0	3	6	V
	Low	VSGL	-9	-8	-7	
Reset gate voltage	High	VRGH	0	3	6	V
	Low	VRGL	-9	-8	-7	
Transfer gate voltage	High	VTGH	0	3	6	V
	Low	VTGL	-9	-8	-7	

Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	0.1	1	MHz
Vertical shift register capacitance	CP1V, CP2V	-	-	6000	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	-	200	-	pF
Summing gate capacitance	CSG	-	-	5	-	pF
Reset gate capacitance	CRG	-	-	5	-	pF
Transfer gate capacitance	CTG	-	-	50	-	pF
Transfer efficiency	CTE	*1	0.99995	0.99999	-	-
DC output level	Vout	*2	12	15	18	V
Output impedance	Zo	*2	-	3	-	kΩ
Power dissipation	P	*2, *3	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*2: The values depend on the load resistance. (VOD=20 V, Load resistance=22 kΩ)
*3: Power dissipation of the on-chip amplifier.

Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × CE	-	V
Full well capacity	Vertical	Fw	-	150	300	-	ke⁻
	Horizontal			-	360	-	
Conversion efficiency		CE	*4	-	3.5	-	μV/e⁻
Dark current (MPP mode)	+25 °C	DS	*5	-	200	3000	e⁻/pixel/s
	0 °C			-	10	150	
Readout noise		Nread	*6	-	4	18	e⁻rms
Dynamic range (Area scanning)		Drange	*7	-	75000	-	-
Spectral response range		λ	-	-	400 to 1100	-	nm
Photoresponse nonuniformity		PRNU	*8	-	-	±10	%
Blemish	Point defects	-	*9	-	-	0	-
	Cluster defects		*10	-	-	0	
	Column defects		*11	-	-	0	

*4: VOD=20 V , Load resistance=22 kΩ
*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*6: -40 °C, operating frequency is 80 kHz.
*7: Drange = Fw / Nread
*8: Measured at half of the full well capacity.
PRNU = noise / signal × 100 [%],
noise: fixed pattern noise (peak to peak)
*9: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels
*10: A group of 2 to 9 continuous point defects
*11: A group of 10 or more continuous point defects

Pin connections (S9736-01)

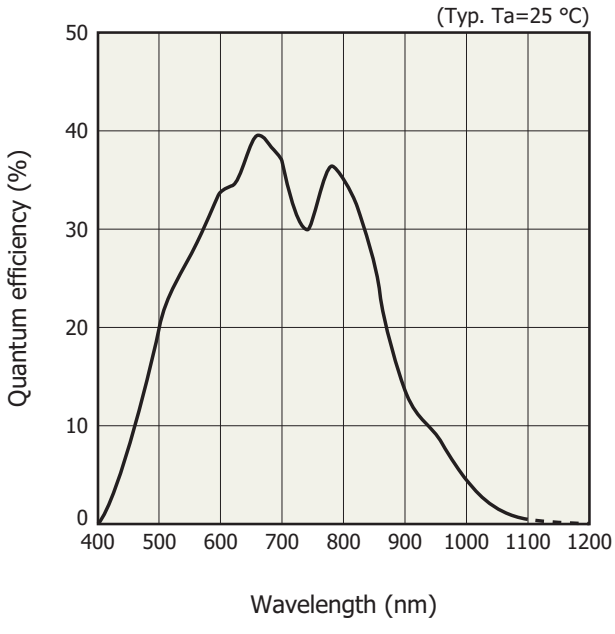
Pin No.	Symbol	Description	Remark
1	RG	Reset gate	-
2	RD	Reset drain	-
3	OS	Output source	-
4	OD	Output transistor drain	-
5	OG	Output gate	-
6	SG	Summing gate	-
7	P2H	CCD horizontal register clock-2	-
8	NC	No connection	-
9	P1H	CCD horizontal register clock-1	-
10	NC	No connection	-
11	IG2H	Test point (horizontal input gate-2)	Shorted to ground
12	IG1H	Test point (horizontal input gate-1)	Shorted to ground
13	ISH	Test point (horizontal input source)	Shorted to RD
14	TG	Transfer gate	-
15	P2V	CCD vertical register clock-2	-
16	NC	No connection	-
17	P1V	CCD vertical register clock-1	-
18	NC	No connection	-
19	NC	No connection	-
20	SS	Substrate (GND)	-
21	NC	No connection	-
22	ISV	Test point (vertical input source)	Shorted to RD
23	IG2V	Test point (vertical input gate-2)	Shorted to ground
24	IG1V	Test point (vertical input gate-1)	Shorted to ground

Pad connections (S9736-03)

Pad No.	Symbol	Description	Remark
1	RG	Reset gate	
2	RD	Reset drain	
3	OS	Output transistor source	
4	OD	Output transistor grain	
5	OG	Output gate	
6	SG	Summing gate	
7	NC		
8	NC		
9	P2H	CCD horizontal register clock-2	
10	P1H	CCD horizontal register clock-1	
11	IG2H	Test point (horizontal input gate-2)	
12	IG1H	Test point (horizontal input gate-1)	
13	ISH	Test point (horizontal input source)	
14	P2V	CCD vertical resister clock-2	
15	P1V	CCD vertical resister clock-1	
16	TG	Transfer gate	Same timing as P2V*12
17	NC		
18	NC		
19	NC		
20	SS	Substrate (GND)	
21	NC		
22	ISV	Test point (vertical input source)	
23	IG2V	Test point (vertical input gate-2)	
24	IG1V	Test point (vertical input gate-1)	

*12: TG is an isolation gate between vertical register and horizontal register.
In standard operation, the same pulse of P2V should be applied to the TG.

Spectral response (without window)



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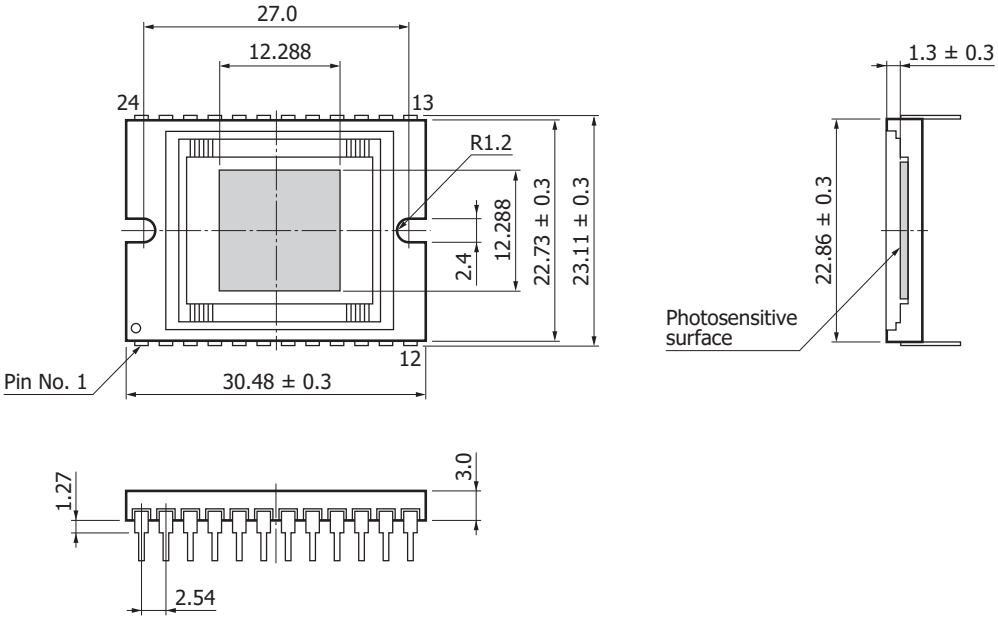
Dimensional outlines (unit: mm)

S9736-01



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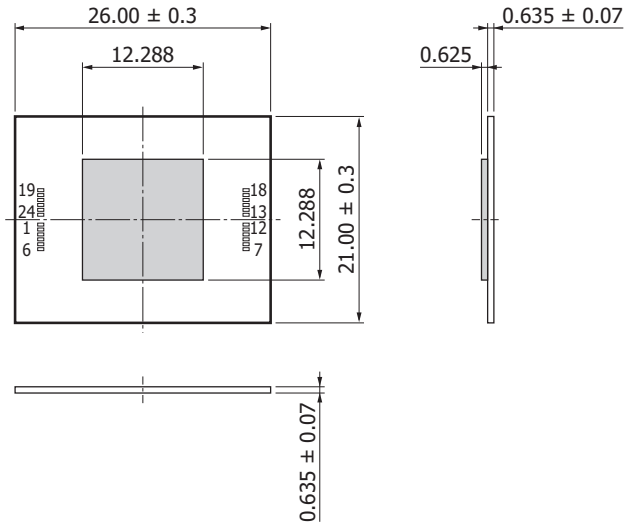
S9736-03



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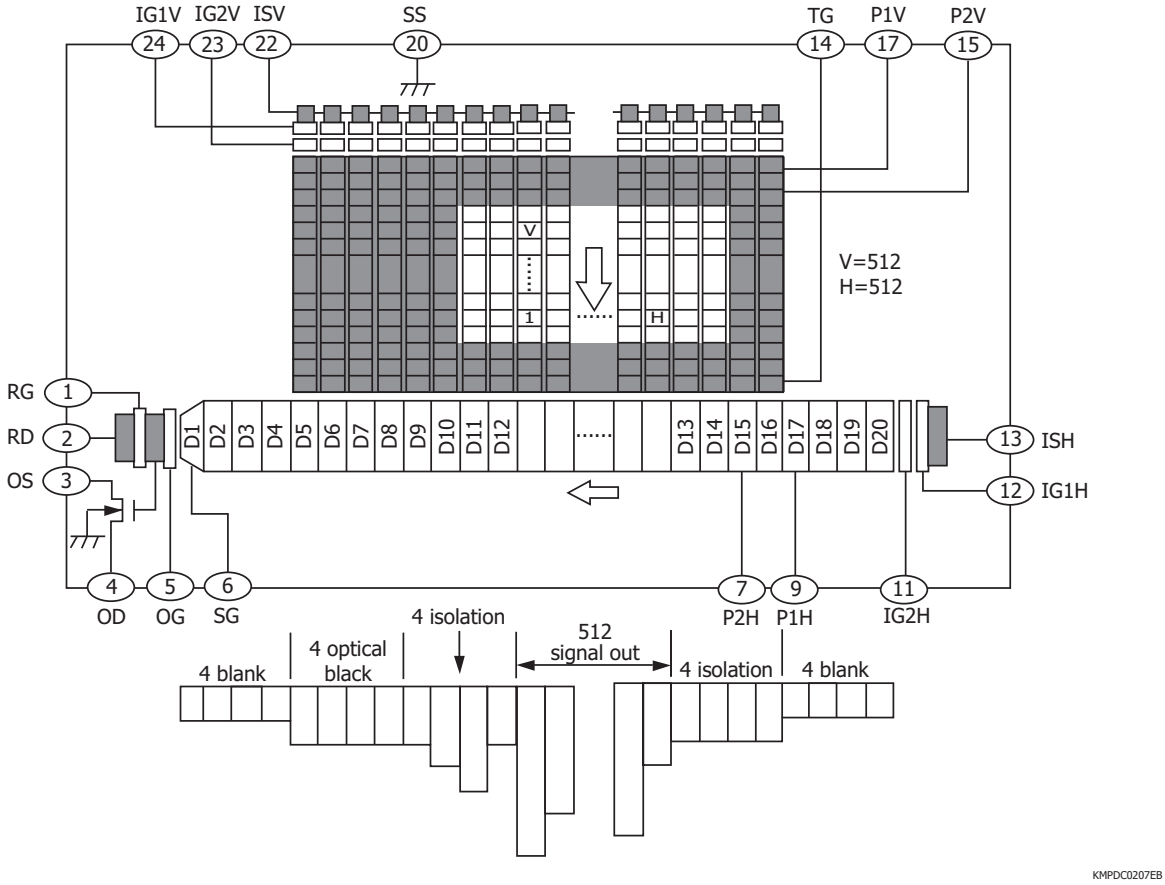
Device structure, line output format (S9736-01)



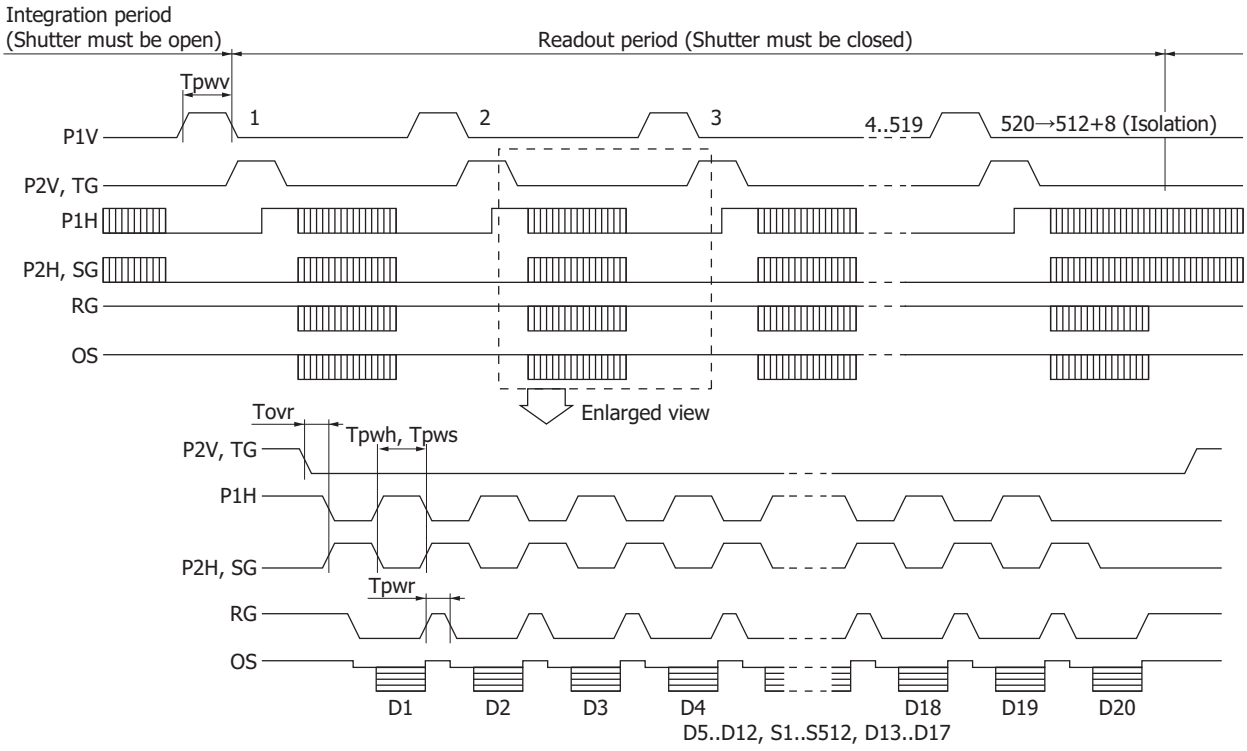
Pixel format

Left ← Horizontal Direction → Right						
Blank	Optical Black	Isolation	Effective	Isolation	Optical Black	Blank
4	4	4	512	4	-	4

Top ← Vertical Direction → Bottom		
Isolation	Effective	Isolation
4	512	4

Timing chart

Area scanning 1 (low dark current mode)



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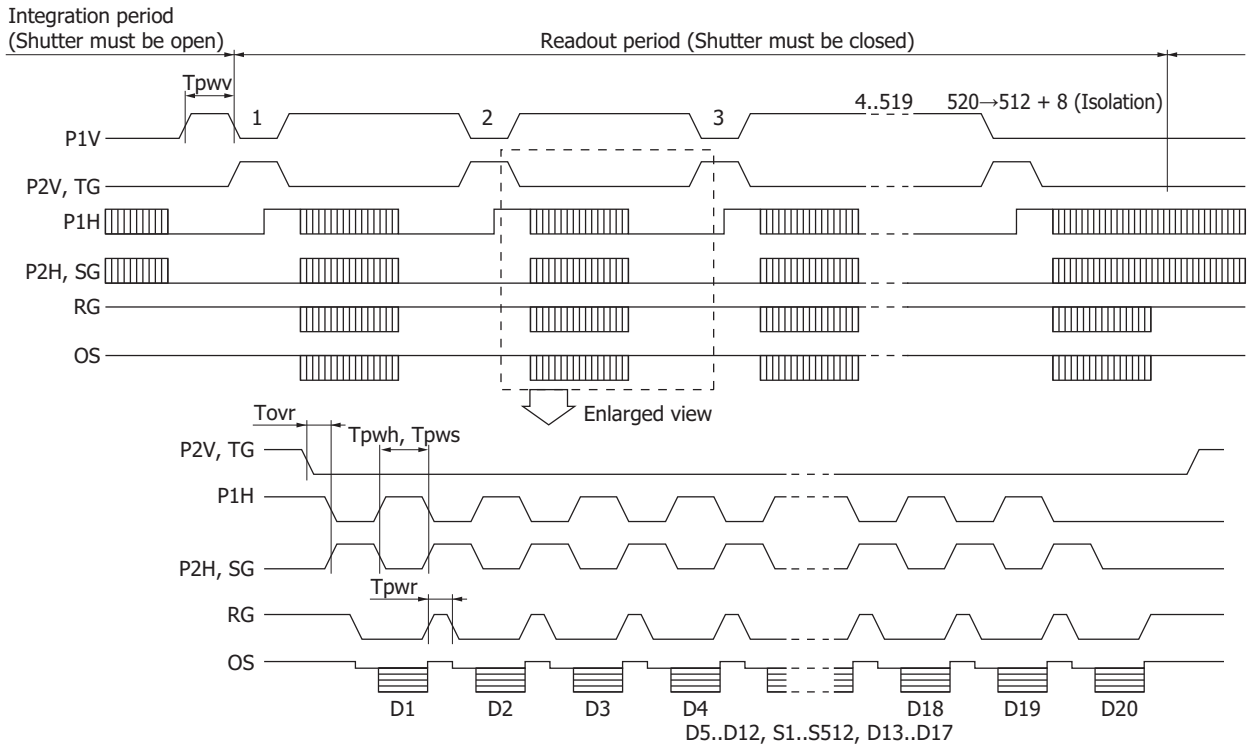
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V P2V, TG	Pulse width	Tpwv	*13	6	18	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*13	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	6	-	µs

*13: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

Area scanning 2 (large full well mode)



KMPDC0209EB

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V P2V, TG	Pulse width	Tpwv	*14	6	18	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*14	500	5000	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	5000	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	500	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	6	-	µs

*14: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

Precautions (electrostatic countermeasures)

· Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
· Do not place these sensors directly on workbenches or floors that may become charged with static electricity.
· Connect a ground wire to workbenches or floors in order to discharge static electricity.
· Ground tools, such as tweezers and soldering irons, that are used to handle these sensors.

It is not always necessary to provide all the electrostatic countermeasures stated above. Implement these countermeasures according to the extent of deterioration or damage that may occur.

Temperature gradient rate for cooling or heating of element

When using an external cooler, set the temperature gradient rate for cooling or heating the element to 5 K/minute or less.

Related information

www.hamamatsu.com/sp/ssd/doc_en.html

■ Precautions
· Disclaimer
· Image sensors

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HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81)53-434-3311, Fax: (81)53-434-5184
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, Bridgewater, N.J. 08807, U.S.A., Telephone: (1)908-231-0960, Fax: (1)908-231-1218, E-mail: usa@hamamatsu.com
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49)8152-375-0, Fax: (49)8152-265-8, E-mail: info@hamamatsu.de
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: (33)1 69 53 71 00, Fax: (33)1 69 53 71 10, E-mail: infos@hamamatsu.fr
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44)1707-294888, Fax: (44)1707-325777, E-mail: info@hamamatsu.co.uk
North Europe: Hamamatsu Photonics Norden AB: Torshamnsgatan 35 16440 Kista, Sweden, Telephone: (46)8-509 031 00, Fax: (46)8-509 031 01, E-mail: info@hamamatsu.se
Italy: Hamamatsu Photonics Italia S.r.l.: Strada della Moia, 1 int. 6, 20020 Arese (Milano), Italy, Telephone: (39)02-93 58 17 33, Fax: (39)02-93 58 17 41, E-mail: info@hamamatsu.it
China: Hamamatsu Photonics (China) Co., Ltd.: B1201, Jiaming Center, No.27 Dongsanhuan Beilu, Chaoyang District, 100020 Beijing, P.R.China, Telephone: (86)10-6586-6006, Fax: (86)10-6586-2866, E-mail: hpc@hamamatsu.com.cn
Taiwan: Hamamatsu Photonics Taiwan Co., Ltd.: 8F-3, No. 158, Section2, Gongdao 5th Road, East District, Hsinchu, 300, Taiwan R.O.C. Telephone: (886)3-659-0080, Fax: (886)3-659-0081, E-mail: info@hamamatsu.com.tw

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