Signetics

27C256/87C256
256K (32K X 8) CMOS UV Erasable PROM

Preliminary Specification

Application Specific Products

FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **87C256-Integrated address latch**
  - **Universal 28-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum CMOS active current**
  - **100μA maximum CMOS standby current**
- **High-performance speeds**
  - **170ns maximum access time**
- **Noise immunity features**
  - **$\pm$ 10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V V_{PP}**

DESCRIPTION

Signetics' 27C256 and 87C256 CMOS EPROMs are 256K-bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 87C256 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

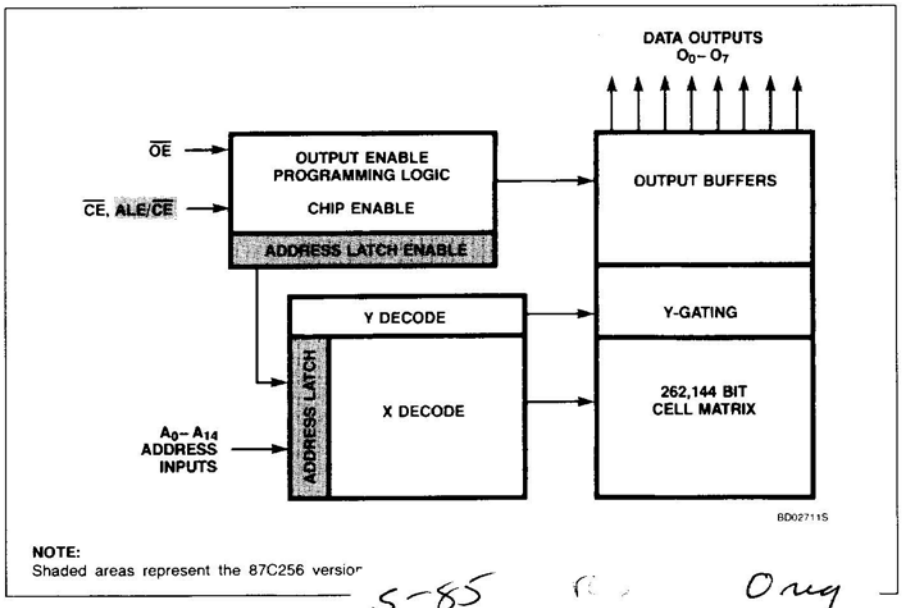
The 27C256 and 87C256 achieve both high-performance (170ns access time for 27C256) and low power consumption (10mA active current maximum, CMOS inputs) making them, ideal for high-performance, portable equipment.

The highest degree of protection against latch-up is achieved through epitaxial processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins from -1V to V_{CC} +1V.

The 87C256 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can tie combined (multiplexed) address-data processor busses directly into both the $A_0 - A_{14}$ and $O_0 - O_7$ pins of the 87C256. During ALE high (ALE/$\overline{CE}$) the address information is allowed to flow into the EPROM and begin accessing the stored code. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs is latched internally. The $A_0 - A_7$ inputs are then ignored as data information is passed on the same bus from the EPROM $O_0 - O_7$ Pins (ALE/$\overline{CE}$ remains low).

The 27C256 and 87C256 are offered in ceramic DIP Packages. Both devices can be programmed with standard EPROM Programmers and the intelligent programming algorithm may be utilized.

BLOCK DIAGRAM



NOTE:
Shaded areas represent the 87C256 version

PIN CONFIGURATION

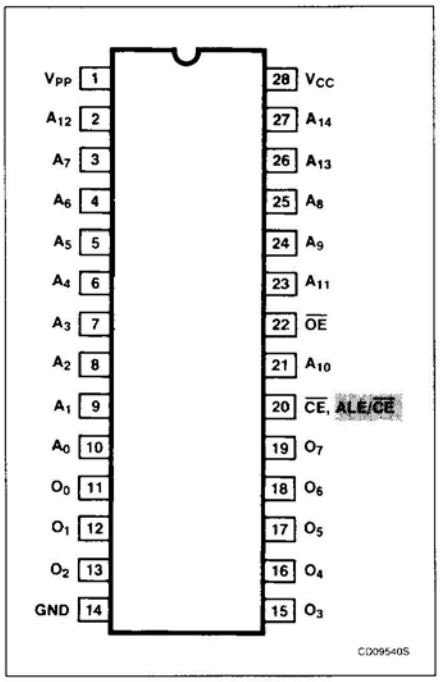


Table 1. Pin Names

$A_0 - A_{14}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
ALE/$\overline{CE}$	Address latch enable/chip enable
GND	Ground
V_{PP}	Program voltage
V_{CC}	Power supply

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